AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of claims:

1. – 8. (Cancelled)

9. (Withdrawn) The method according to claim 1, further comprising XORing corresponding register bit locations in each one of said plurality of semaphore registers.

10. (Withdrawn) The method according to claim 9, further comprising addressing each one of said register bit locations by coupling at least one XOR gate utilized for said XORing to a bit line in said limited-width test bus.

11. – 17. (Cancelled)

18. (Withdrawn) The method according to claim 13, further comprising determining a software thread identifier by XORing corresponding register bit locations in each one of said plurality of semaphore registers.

19. – 24. (Cancelled)

25. (Withdrawn) The system according to claim 19, wherein corresponding register bit locations in each one of said plurality of semaphore registers are coupled to an XOR gate.

26. (Withdrawn) The system according to claim 25, wherein each said XOR gate is coupled to a bit line in said limited-width test bus.

27. – 33. (Cancelled)

34. (Previously Presented) A method for sharing hardware resources in a digital system, the method comprising:

determining whether a hardware resource is in use by monitoring contents of at least one of a plurality of semaphore registers;

accessing said monitored contents of said plurality of semaphore registers by using a limited-width test bus whose bus width contains less than a number of bits needed to individually address each of said plurality of semaphore registers; and

XORing corresponding register bit locations in each one of said plurality of semaphore registers.

35. (Previously Presented) A method for sharing hardware resources in a digital system, the method comprising:

determining whether a hardware resource is in use by monitoring contents of at least one of a plurality of semaphore registers;

accessing said monitored contents of said plurality of semaphore registers by using a limited-width test bus whose bus width contains less than a number of bits needed to individually address each of said plurality of semaphore registers;

XORing corresponding register bit locations in each one of said plurality of semaphore registers; and

addressing each one of said register bit locations by coupling at least one XOR gate utilized for said XORing to a bit line in said limited-width test bus.

36. (Previously Presented) A method for sharing hardware resources in a digital system, the method comprising:

arranging a plurality of semaphore registers into a plurality of semaphore register blocks;

selecting one of said plurality of semaphore register blocks to be accessed by a limited-width test bus; and

determining a software thread identifier by XORing corresponding register bit locations in each one of said plurality of semaphore registers.

37. (Previously Presented) A system for sharing hardware resources in a digital system, the system comprising:

a plurality of hardware resources;

a plurality of semaphore registers coupled to said plurality of hardware resources; and

a limited-wldth test bus coupled to said plurality of semaphore registers, wherein said limited-width test bus contains less than a number of bits needed to individually address each of said plurality of semaphore registers and corresponding register bit locations in each one of said plurality of semaphore registers are coupled to an XOR gate.

38. (Previously Presented) A system for sharing hardware resources in a digital system, the system comprising:

a plurality of hardware resources;

a plurality of semaphore registers coupled to said plurality of hardware resources; and

a limited-width test bus coupled to said plurality of semaphore registers, wherein said limited-width test bus contains less than a number of bits needed to individually address each of said plurality of semaphore registers, corresponding register bit locations in each one of said plurality of semaphore registers are coupled to an XOR gate, and each said XOR gate is coupled to a bit line in said limited-width test bus.